

REQUEST FOR RECONSIDERATION

Claims 1-18 are pending in the application. Claims 1-8 and 10-18 are rejected. Claim 9 is objected to. Applicant respectfully requests reconsideration and allowance of all pending claims.

Dependent claims 19 and 20 have been added to further define the invention. No new matter has been added and it is believed that no new search is required.

Objection of Drawings

The Office Action objected to FIGURE 9 because it did not show "945" described on page 7, line 23. In response to the objection, the applicant has corrected FIGURE 9. Attached to this response is both a clean copy of FIGURE 9 as corrected, and a marked version of FIGURE 9 showing the corrections.

The drawings were also objected to because it is believed that the connections of the P-channel transistors of FIGURES 3, 9, and 10 are incorrect. The P-channel transistors illustrated within the figures are P-channel FETs (See Specification, Page 6, line 10, Page 7, Lines 11-12). Therefore, FIGURES 3, 9, and 10 are correct as illustrated. For further clarification please see discussion under the Objection to Specification section.

Objection to Specification

The Office Action requested clarification with respect to the operation of the circuit with respect to transistor M1 of FIGURE 3. As illustrated in FIGURE 3, transistor M1 is a P-channel FET (See Specification, Page 6, Line 10) and can operate in either direction. The arrow on the

transistor is used to indicate where the body is connected. This body connection is illustrated in FIGURE 4. The P-channel FETs illustrated in the other figures operate in the same manner. Therefore, it is believed that the operation of the transistors has been clarified with regard to the rest of the figures.

The Office Action also requested clarification with regard to transistors M1 and M2 being replaced by a single diode (See Specification, Page 7, Lines 10-11). This is the correct interpretation. Transistors M1 and M2 may be replaced by a single diode.

The Office Action believed that transistors M91 and M92 on page 9, line 25 of the specification should be M101, M102, M103, and M104 to correspond to the transistors shown in FIGURE 10. An amendment to the specification has been made to incorporate the change.

Rejection of Claims under 35 U.S.C. §112

Claims 1-7 and 14 are rejected in the Office Action under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. According to the Office Action, "Claim 1, lines 4-5 are misleading because they indicate the charge storage circuit receives the first signal and also outputs the second signal during a transient event. However, doesn't the charge storage circuit only receive the first signal when the signal transfer circuit is conducting?" (Office Action, Page 4, 1st paragraph) The Applicant respectfully submits that claim 1, as amended, meets the requirements of 35 U.S.C. §112. As amended, Claim 1 recites, in part, that "the charge storage circuit arranged to receive the first signal during normal operation."

The Office action rejected claims 11 and 12 because of insufficient antecedent basis. The Applicant respectfully submits that claims 11 and 12, as amended, meet the requirements of 35 U.S.C. §112.

The Office Action rejected claim 14 "as being incomplete for omitting essential structural cooperative relationships of elements...The omitted structural cooperative relationships are how the complementary switch and charge storage circuit relate to one another." (Office Action, Page 4, 3rd paragraph) The Applicant respectfully submits that claim 14, as amended, meets the requirements of 35 U.S.C. §112.

Rejection of Claims under 35 U.S.C. §103(a)

Claims 1-6, 8, 10-12, 17, and 18 are rejected by the Office Action under 35 U.S.C. 103(a) as being unpatentable over Tailliet. The Office action states that it would be obvious to one of ordinary skill in the art that circuit 3 in Fig. 2 of Tailliet "would be protected from a sudden short, transient event, thus rendering claims 1 and 2 obvious." (Office Action, Pages 5, 6) Applicant respectfully disagrees. The Office Action even states that "the reference does not clearly describe normal and transient event operations." (Office action, Page 5, last paragraph). Tailliet uses capacitor C2 to aid in detection of a POR, not to provide power to a pin of a circuit (See Tailliet, Column 6, lines 14-17). As amended claim 1 recites, in part, that the charge storage circuit is arranged to "output a second signal that provides power during the transient event to the pin of the circuit." The cited reference does not include this limitation and cannot achieve the operation of the Applicant's invention. Therefore, claim 1 is novel and non-obvious in view of the cited art. Accordingly, claim 1 is patentable over the cited references.

For at least the reasons discussed above, applicant respectfully submits that independent Claims 8, 17, and 18, as amended, are not obvious in view of the references cited in the Office Action and are, therefore, allowable. Claims 2-6 and 9-13, are dependent from valid base claims, and therefore include the limitations of the base claims. Therefore, Claims 2-6 and 9-13 are allowable for at least the same reasons.

Objection of Claims

Claims 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Office Action also states that claim 7 and claims 13-16 would be allowable if rewritten to overcome the §112 rejections and to include the limitations of the base claim and any intervening claims.

Claim 14 has been amended to overcome the §112 rejection. Applicant believes that claim 14 is allowable as amended. Thus, Claims 15-16 should also be allowable since they depend on a valid base claim.

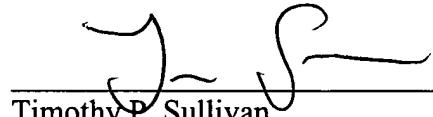
Conclusion

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

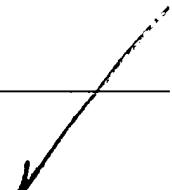
Attached to this response are pages entitled "MARKED VERSION SHOWING CHANGES" that illustrate the changes made to the paragraphs and claims amended above. Also attached to this response is a clean copy of FIGURE 9 as corrected, and a marked version of FIGURE 9 showing the corrections.

Respectfully Submitted,

MERCHANT & GOULD P.C.



Timothy P. Sullivan
Registration No. 47,981
Direct Line: 206.342.6254



TPS/sml



MARKED VERSIONS SHOWING CHANGES

In the Specification:

Please substitute the following for the paragraph on page 9, lines 22-26:

--It will be appreciated in view of the present disclosure that transistors M101, M102, M103, and M104 may be NPN transistors, PNP transistors, Bipolar devices, MOS devices, GaAsFET devices, JFET devices, as well as one or more components that are arranged to provide the function of transistors [M91 and M92] M101, M102, M103, and M104 in the above described example.—

In the Claims:

Claims 19 and 20 have been added.

Please amend Claims 1, 8, 11, 12, 14, 17, and 18 as shown:

1. (Amended) An apparatus for protecting a circuit from a transient event, comprising:

a signal transfer circuit arranged to receive a supply signal and output a first signal during normal operation to a pin of the circuit and to a charge storage circuit,

the charge storage circuit arranged to receive the first signal during normal operation and output a second signal to provide power during the transient event to the pin of the circuit, the charge storage circuit storing enough charge to provide the second signal during the transient event.

8. (Amended) An apparatus for protecting a circuit from a transient event, comprising:

a signal transfer circuit arranged to receive a supply signal and output a first signal during normal operation;

a charge storage circuit arranged to receive a bias signal and the first signal, the charge storage circuit providing a second signal that provides power during the transient event; and

RECEIVED
TECHNICAL CENTER 2800
OCT 24 2002

an inverting circuit arranged to receive the first signal, second signal, and the bias signal, the inverting circuit coupled to a pin of the circuit, the inverting circuit arranged to hold the pin of the circuit high during a startup of the circuit, and low during the transient event and during normal operation.

11. (Amended) The apparatus of Claim 8, wherein the [storage] signal transfer circuit is a diode circuit.

12. (Amended) The apparatus of Claim 8, wherein the [storage] signal transfer circuit is a transistor circuit.

14. (Amended) An apparatus for protecting a logic pin of a circuit from changing logic states during a transient event, comprising:

a complementary switch that is arranged to receive an input logic signal and output an output logic signal during normal operation; and

a charge storage circuit coupled to the complementary switch and arranged to provide a secondary logic signal during the transient event.

17. (Amended) A method for rejecting a transient event from a circuit, comprising:
receiving a supply signal;
monitoring the supply signal for the transient event;
determining when the circuit is in normal operation, and when the transient event is occurring:

providing a first signal from a signal transfer circuit to a pin of the circuit when it is determined that the circuit is in normal operation, and

providing a second signal from a charge storage circuit that provides power to the pin of the circuit when it is determined that the transient event is occurring.

18. (Amended) An apparatus for protecting a pin of a circuit during a transient event, comprising:
a means for receiving a supply signal;
a means for monitoring the supply signal to determine the transient event;
a means for determining when the circuit is in normal operation and when the transient event is occurring:

a means for providing a first signal from a signal transfer circuit to a pin of the circuit when it is determined that the circuit is in normal operation, and

a means for providing a second signal from a charge storage circuit that provides power to the pin of the circuit when it is determined that the transient event is occurring.